RZ/A2M Group

RZ/A2M CACHE Driver

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Introduction

This application note describes the operation of the software CACHE Driver for the RZ/A2 device on the RZ/A2M CPU Board.

It provides a comprehensive overview of the driver. For further details please refer to the software driver itself.

The user is assumed to have knowledge of e^2 studio and to be equipped with an RZ/A2M CPU Board.

Target Device

RZ/A2M Group

Driver Dependencies

This driver has no other driver dependencies.

Referenced Documents

Document Type	Document Name	Document No.
User's Manual	RZ/A2M Hardware Manual	R01UH0746EJ

List of Abbreviations and Acronyms

Abbreviation	Full Form
API	Application Programming Interface
ARM	Advanced RISC Machines
CPU	Central Processing Unit
IDE	Integrated Development Environment
LLD	Low Layer Driver

Table 1-1 List of Abbreviations and Acronyms

Contents

1. Outline of Software Driver

The CACHE (L1/L2 cache) driver is an abstraction layer between the application and the hardware. It provides an API for controlling both the L1 and L2 cache. Functions are provided for various operations, such as initialising the cache, enabling and disabling the cache, invalidating and clearing the cache, etc.

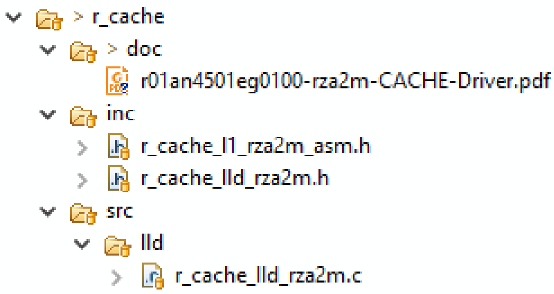
2. Description of the Software Driver

The key features of the driver include:

- Control of both the Level 1 (L1) and Level 2 (L2) caches
- The ability to enable and disable each cache
- Invalidating and cleaning all or part of each cache

2.1 Structure

Unlike many of the other drivers, the CACHE driver currently consists of a single layer: the Low Layer Driver (LLD). This includes all the hardware specific functions and provides the API to the application.



2.2 Description of each file

Each file's description can be seen in the following table.

Filename	Usage	Description
Low Layer API		
r_cache_lld_xxxx.h	API header file	Low Layer Driver (LLD) header file (where "xxxx" is a device and board-specific identification). This is the header file to include in application code.
r_cache_l1_xxxx_asm.h	Private LLD header file	Defines functions used within the driver
Low Layer Driver (LLD) Source		
r_cache_lld_xxxx.c	Private (LLD only)	(Where "xxxx" is a device and board specific identification). Provides the function definitions for the Low Layer Driver interface.

2.3 Low Layer Driver

The Low Layer Driver provides the functions to configure the hardware.

Return Type	Function	Description	Arguments	Return
void	**R_CACHE_L1Init**(void)	Initialise the Cortex-A9 L1 cache	None	None
void	**R_CACHE_L1InstInvalidAll**(void)	Invalidate whole of the Cortex-A9 L1 instruction cache	None	None
void	**R_CACHE_L1DataInvalidAll**(void)	Invalidate whole of the Cortex-A9 L1 data cache	None	None
void	**R_CACHE_L1DataCleanAll**(void)	Clean whole of the Cortex-A9 data cache	None	None
void	**R_CACHE_L1DataCleanInvalidAll**(void)	Clean and invalidate whole of the Cortex-A9 L1 data cache	None	None
e_err_code_t	**R_CACHE_L1DataInvalidLine**(void * line_addr, uint32_t size)	Invalidate the L1 cache lines that are included in the specified address range	**line_addr:** [in] virtual start address **size:** [in] size in bytes from line_addr	**DRV_SUCCESS or DRV_ERROR**
e_err_code_t	**R_CACHE_L1DataCleanLine**(void * line_addr, uint32_t size)	Clean the L1 cache lines that are included in the specified address range	**line_addr:** [in] virtual start address **size:** [in] size in bytes from line_addr	**DRV_SUCCESS or DRV_ERROR**
e_err_code_t	**R_CACHE_L1DataCleanInvalidLine**(void * line_addr, uint32_t size)	Invalidate and clean the L1 cache lines that are included in the specified address range	**line_addr:** [in] virtual start address **size:** [in] size in bytes from line_addr	**DRV_SUCCESS or DRV_ERROR**
void	**R_CACHE_L1InstEnable**(void)	Enable the Cortex-A9 L1 instruction cache	None	None
void	**R_CACHE_L1InstDisable**(void)	Disable the Cortex-A9 L1 instruction cache	None	None
void	**R_CACHE_L1DataEnable**(void)	Enable the Cortex-A9 L1 data cache	None	None
void	**R_CACHE_L1DataDisable**(void)	Disable the Cortex-A9 L1 data cache	None	None
void	**R_CACHE_L1BtacEnable**(void)	Enable the Cortex-A9 branch prediction	None	None

void	**R_CACHE_L1BtacDisable(void)**	Disable the Cortex-A9 branch prediction	None	None
void	**R_CACHE_L1BtacInvalidate(void)**	Invalidate the Cortex-A9 branch predictor	None	None
void	**R_CACHE_L1PrefetchEnable(void)**	Enable the Cortex-A9 instruction and data prefetching	None	None
void	**R_CACHE_L1PrefetchDisable(void)**	Disable the Cortex-A9 instruction and data prefetching	None	None
void	**R_CACHE_L2Init(void)**	Initialise the PL310 L2 cache controller	None	None
void	**R_CACHE_L2CacheEnable(void)**	Enable the PL310 L2 cache	None	None
void	**R_CACHE_L2CacheDisable(void)**	Disable the PL310 L2 cache	None	None
void	**R_CACHE_L2PrefetchEnable(void)**	Enable the PL310 L2 cache instruction and data prefetching	None	None
void	**R_CACHE_L2PrefetchDisable(void)**	Disable the PL310 L2 cache instruction and data prefetching	None	None
void	**R_CACHE_L2InvalidAll(void)**	Invalidate the entire PL310 L2 cache	None	None
void	**R_CACHE_L2CleanAll(void)**	Clean the entire PL310 L2 cache	None	None
void	**R_CACHE_L2CleanInvalidAll(void)**	Clean and invalidate the entire PL310 L2 cache	None	None
uint32_t	**R_CACHE_GetVersion(st_drv_info_t *pinfo)**	Get Low Layer Driver version information	**pinfo**: [out] pointer to version information structure	**DRV_SUCCESS**

3. Example of Use

This section gives simple examples for initialising and using the driver, and for getting the driver version.

3.1 Initialise the L1 Cache

```
R_CACHE_L1Init();
```

3.2 Initialise the L2 Cache

```
R_CACHE_L2Init();
```

3.3 Clean and Invalidate the Entire L1 Data Cache

```
R_CACHE_L1DataCleanInvalidAll();
```

3.4 Invalidate the Entire L1 Instruction Cache

```
R_CACHE_L1InstInvalidAll();
```

3.5 Enable the L1 Instruction Cache

```
R_CACHE_L1InstEnable();
```

3.6 Enable the L1 Data Cache

```
R_CACHE_L1DataEnable();
```

3.7 Get Version

```
st_drv_info_t info;
uint32_t result;

result = R_CACHE_GetVersion(&info);
```

4. OS Support

This driver supports any OS.

5. How to Import the Driver

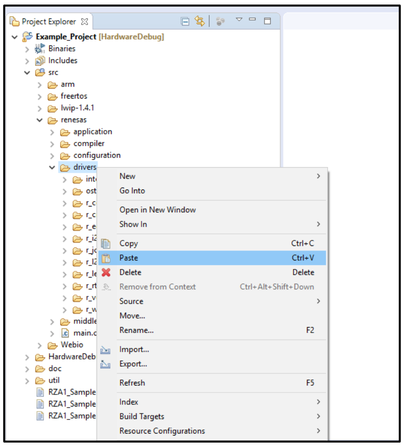
This section describes how to import the driver into your project. Generally, there are two steps in any IDE:

1) Copy the software driver to the location in the source tree that you require for your project.
2) Add the include path of the driver to the compiler.

5.1 e² studio

To import the driver into your project please follow the instructions below.

1) In Windows Explorer, right-click on the r_cache folder, and click **Copy**.
2) In e² studio Project Explorer view, select the folder where you wish the driver project to be located; right-click and click **Paste**.
3) Right-click on the parent project folder (in this case 'Example_Project') and click **Properties ...**
4) In 'C/C++ Build → Settings → Cross ARM Compiler → Includes', add the include folder of the newly added driver, e.g. '${ProjDirPath}\src\renesas\drivers\r_cache\inc'



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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Sept 19, 2018	All	Created document.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   ¾ The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   ¾ The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   ¾ The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   ¾ When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   ¾ The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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